REDUCTION OF OFFSET AND LOW VOLTAGE OF DYNAMIC COMPARATOR FOR ADCs

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ABSTRACT

A low-offset dynamic comparator using new dynamic offset cancellation technique is proposed. The technology scaling of MOS transistors enables low voltage and low power which decreases the offset voltage and delay of the comparator. The new technique achieves low offset and low voltage without pre-amplifier. Furthermore the overdrive voltage of the input transistor can be optimized to reduce the offset voltage of the comparator independent of the input common mode voltage. The input transistor drain nodes and use of buffers at the output nodes can further reduce the offset. The modifications made to the typical differential pair dynamic comparator will be reducing the overall offset voltage. Moreover, the proposed comparator has an advantage that the offset voltage does not change by increasing the input common mode voltage compared with the conventional comparator. By implementing this in dynamic comparator technique a low voltage and offset voltage can be achieved.

Keywords : Analog to digital converter (ADC),Offset voltage,delay, latch comparator.

1.INTRODUCTION

Analog-to-digital converters (ADC) have become a significant element driving the semiconductor industry over the past few years. Small size processes, low power indulgences, increased integration of different functional blocks within a single chip and a reduced propagation delay make them more acceptable to the semiconductor industry and they are able to provide high speed with low power dissipation.

Comparators are the most widely used electronic components next to operational amplifiers in electronic systems. Comparators are also performed as 1-bit analog-to-digital converter and for that reason they are mostly used in large number of A/D converter. The applications of the comparators are zero-crossing detectors, peak detectors, switching power regulators, BLDC operating motors, data transmission, and others. The outputs are binary signal based on comparison.

The schematic symbol and basic operation of a voltage comparator are shown in figure.1. VP is the input voltage (Pulse voltage) applied to the positive input terminal of comparator and Vn is the reference voltage (constant DC voltage) applied to the negative terminal of comparator. Now if pulse voltage(VP), the input of the comparator is at a greater potential than the reference voltage (Vn), the reference voltage, then the output of the comparator is logic1, where as if the VP is at a potential less than the Vn, the output of the comparator is at logic 0.

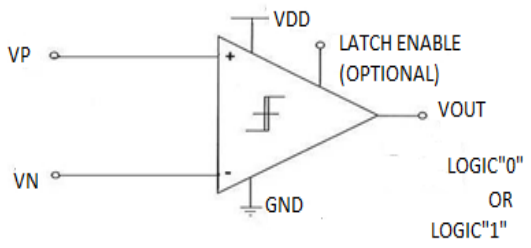

Figure 1. Schematic diagram of the comparator

In conventional designs, we used pre-amplifiers for offset- voltage cancellation (1) but it increases power consumption due to wide bandwidth amplifier are required to reduce the offset-voltage in the high frequency operation.

Furthermore it is very difficult to realize a high voltage gain amplifier because of low drain resistance caused by scaling. Therefore we strongly required a technique to reduce the offset-voltage without using amplifier. In recent years, some offset-voltage cancellation techniques were proposed. In reference (2), load capacitances used in the comparator are controlled digitally to reduce the offset-voltage. The resolution of the calibration is determined by the size of the load capacitance and the digital word but it gives a high resolution ADC with lower speed and wider area.

In conventional CMOS comparator designs, the preamplifier is typically followed by a standard dynamic CMOS latch. As shown in the following subsection, this latch has a potentially large input offset and therefore requires the use of a high-gain preamplifier in order to achieve a low offset.

2.CONVENTIONAL COMPARATOR

All the transistors should be properly matched in layout and biased in the saturation region to make a dynamic latch comparator more vigorous against mismatch and process variations. A fully differential dynamic latch comparator based on cross-coupled differential pairs. Designing high-speed comparators is more challenging when the supply voltage is smaller. In figure.2. a given technology, to achieve high speed, larger transistors are required to compensate the reduction of supply voltage, which also means that more die area and power is needed. The accuracy of comparators is mainly defined by its offset value, along with power consumption, speed has more importance in achieving overall higher performance of ADCs[11]. This can be achieved by the fully dynamic latched Comparator. This comparator shows 14.6mV offset which is small [9] when compared to other dynamic comparators and preamplifier based comparators.

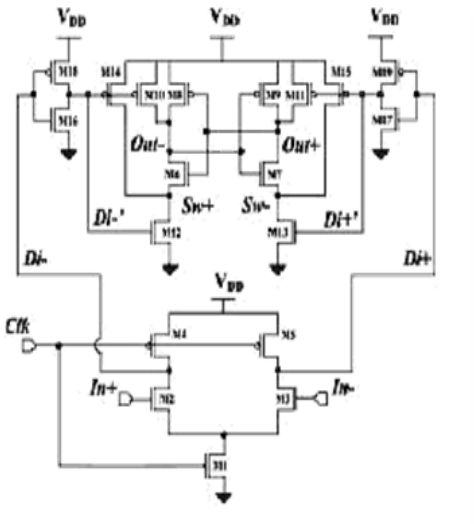

Figure 2. Conventional comparator

3.DYNAMIC COMPARATOR

The dynamic comparator latch circuit is separated from the amplification branches[1]. Each stage operates independently with different clock pulses, ˜1 and ˜2. This separation helps the input transistors to overcome the mismatch effect.

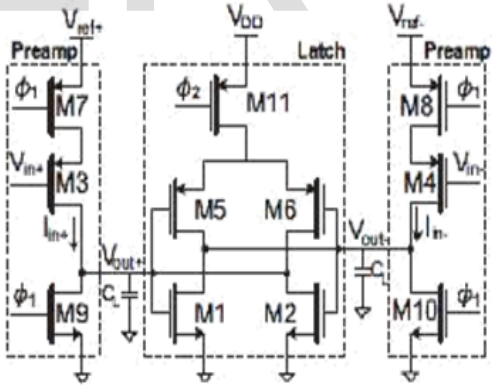

Figure 3. Dynamic comparator

Inside the latch circuit before the offset of the latch circuitry is involved in the overall decision making process [13]. Hence, it significantly reduces the input referred offset voltage of the comparator.

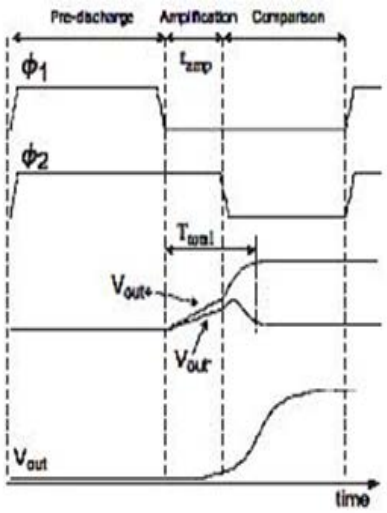

Figure 4. Conceptual waveform

The proposed comparator [10] works with a special three phase signaling. The signal waveform of the comparator is illustrated in Figure.3.At the first phase or pre-charging phase both ˜1 and ˜2 are high. Therefore, the cross coupled inverter pairs are off and pre-charge transistors discharge the output nodes to the ground. The second phase or the amplification phase will occur when ˜1 is low and ˜2 is still high[7]. Consequently, the path to the ground is cut while the reference voltages can feed the input branch and let the input cascade transistors conduct[12]. The difference between the amount of the current produced in the input branches, I_{in+}- I_{in-} , is related to the voltage difference between the input and the reference differential voltage.

During the amplification phase, the currents set the differential voltage at the internal nodes of the cross-couple latch, Vout+ and Vout-. In the third phase, the comparison phase, the latch circuit operates and the induced differential voltage is boosted in the regenerative loop of the cross-coupled inverters.

4.PROPOSED COMPARATOR

The main concept of the proposed technique is to cancel the offset of the preamplifier through adjusting the body voltages of the input transistors. Offset cancellation is performed in foreground during which the normal operation of the ADC is interrupted. During the offset-cancellation cycle, the common-mode voltage Vcm is applied to both input transistors of the preamplifier.

Due to the fact that the preamplifier offset has prominent effect on the total equivalent input-referred offset voltage, cancelling it will lead to significant reduction in the total input-referred offset, as far as the effect of the latch offset is greatly reduced by the gain of the preamplifier. Since the threshold voltage, Vth, changes with the source-body voltage, VSB, and the transistor current changes with Vth, offset calibration is performed by modifying the body voltages of the input transistors, M1 & M2.

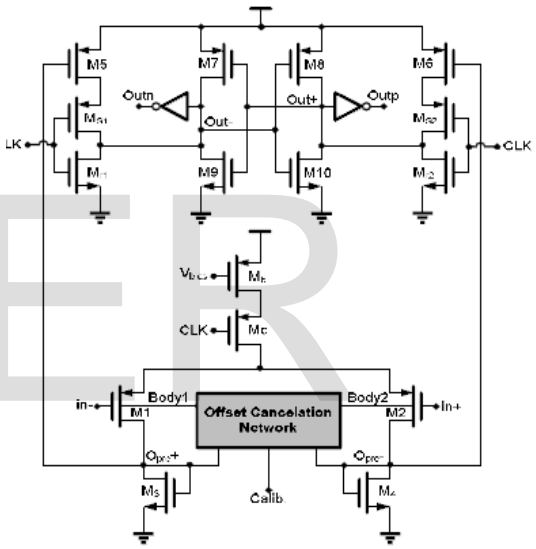

Figure 5. Proposed dynamic comparator

The operation of the comparator is as follows. When the clock is at Vdd, the outputs of the latch are reset to ground (by Mr1 –Mr2), also transistors Ms1-Ms2 disconnect the latch from the preamplifier in order to avoid kickback noise and hysteresis. The gain of the preamplifier has been chosen equal to 3, in order to reduce the input referred latch offset voltage below the acceptable value of 1VLSB.

Besides, the preamplifier tail transistor (Mc) is cut-off to prevent any static current from the supply to ground. When the clock becomes low, Mc is turned on and the input transistors force the current into diode-connected loads (M3-M4). Any mismatch between the input

transistors contribute the most in the preamplifier total offset as far as they control the currents to the loads. Based on the output voltage of the preamplifier, regeneration begins in the latch and the outputs are set to Vdd and ground.

5.IMPLEMENTATION

To compare the performances of the proposed comparator with the previous works. Each circuit here was designed using 0.25ìm technology, frequency at 25MHZ is simulated at Tanner 13 version.

5.1.Conventional Comparator

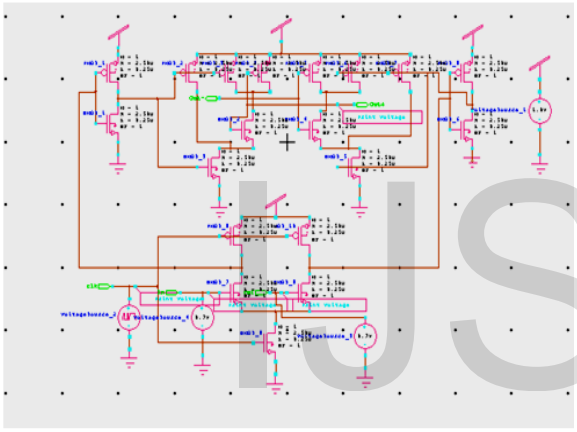

Figure 6. Schematic design of conventional comparator

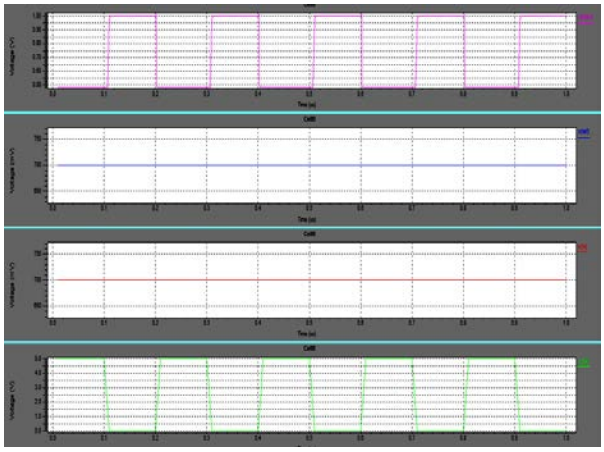

Figure 7. Transient response of conventional comparator

5.2.Dynamic Comparator

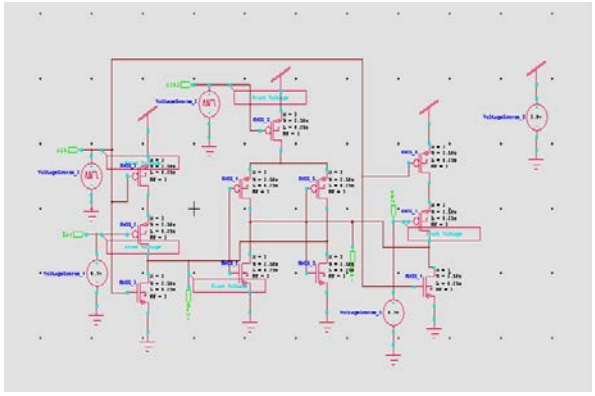

Figure 8. Schematic design of dynamic comparator

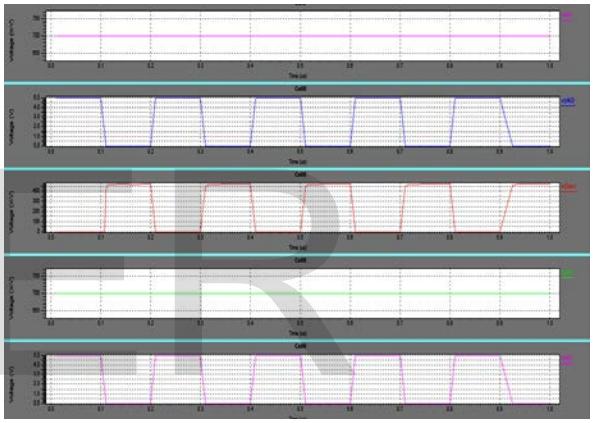

Figure 9. Transient response of dynamic comparator

5.3.Proposed Dynamic Comparator

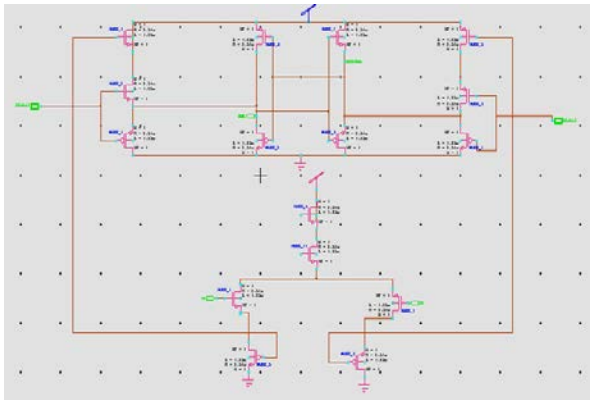

Figure 10. Schematic design of proposed dynamic comparator

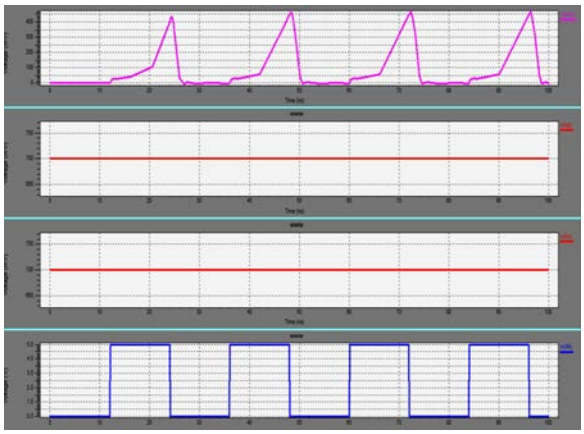

Figure 11. . Transient response of proposed dynamic comparator

6. EXPERIMENTAL RESULTS

The following table shows the various result obtained using the Tanner tool

Table 1: Number Of Transistor Used In Each Comparator

Comparator	Number of transistor
Existing comparator	19
Proposed	16

The following table shows the offset voltage of various comparators

Table 2: Offset Voltage Of Each Comparator

Comparator	Offset voltage
Existing comparator	14.6mV
Proposed	750µV

CONCLUSION

The results are simulated in Tanner with 0.25ηm technology. A new analog-based offset cancellation technique based on body-voltage trimming has been presented. The simple architecture of the offset cancellation network avoids any design complexity, capacitive loading or power-consumed. Offset voltage is reduced using a offset cancellation technique and Delay will also be reduced compared with existing dynamic comparator.

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